WHAT IS CLAIMED IS:

1. A synchronous signal producing circuit for synchronizing access by a processor and a coprocessor to a shared memory, comprising:

an access inhibit region register for designating an access inhibit region for said processor in said shared memory;

a comparing circuit for detecting the access by said processor to said access inhibit region designated in said access inhibit region register; and

a first logic circuit for issuing a signal setting said processor to a wait state based on a signal indicating that said coprocessor is executing a coprocessor instruction as well as a result of the comparison by said comparing circuit.

2. The synchronous signal producing circuit according to claim 1, wherein

said first logic circuit issues the signal setting said processor to the wait state based on the signal indicating that said coprocessor is executing the coprocessor instruction, the result of the comparison by said comparing circuit and a signal indicating that locking of said shared memory is to be released.

3. The synchronous signal producing circuit according to claim 1, further comprising:

a bus wait counter for counting the number of bus wait cycles; and

a second logic circuit for issuing a bus error signal to said processor based on the signal indicating that said coprocessor is executing the coprocessor instruction, the result of the comparison by said comparing circuit and a count value of said bus wait counter.

4. The synchronous signal producing circuit according to claim 1, further comprising:

a first initial value register for setting a wait number at the time when the signal issued by said first logic circuit sets said processor to the

wait state;

a second initial value register for setting a wait number at the time of normal access by said processor;

a selector for selecting the values in said first and second initial value registers based on the signal indicating that said coprocessor is executing the coprocessor instruction as well as the result of the comparison by said comparing circuit; and

a bus wait counter for receiving the value selected by said selector, and issuing a bus error signal to said processor when said bus wait counter counts the selected value.

5. The synchronous signal producing circuit according to claim 1, further comprising:

a third logic circuit for issuing a signal setting said processor to a low power consumption mode based on the signal indicating that said coprocessor is executing the coprocessor instruction as well as the result of the comparison by said comparing circuit.

6. The synchronous signal producing circuit according to claim 1, further comprising:

a coprocessor instruction execution flag for holding information indicating that the said coprocessor is executing the coprocessor instruction, wherein

said first logic circuit issues a signal for setting said processor to the wait state based on the information held in said coprocessor instruction execution flag and the result of the comparison by said comparing circuit.

7. The synchronous signal producing circuit according to claim 6, wherein

said access inhibit region register includes a first access inhibit region register for designating a first access inhibit region for said processor in said shared memory, and a second access inhibit region register for designating a second access inhibit region for said processor in said shared

memory

said comparing circuit includes a first comparing circuit for detecting the access by said processor to said first access inhibit region designated in said first access inhibit region register, and a second comparing circuit for detecting the access by said processor to said second access inhibit region designated in said second access inhibit region register;

said coprocessor instruction execution flag includes a first coprocessor instruction execution flag for holding information indicating that the said coprocessor is executing the coprocessor instruction, and a second coprocessor instruction execution flag; and

said first logic circuit includes a second logic circuit issuing a signal for setting said processor to the wait state based on the information held in said first coprocessor instruction execution flag and the result of the comparison by said first comparing circuit, and a third logic circuit issuing a signal for setting said processor to the wait state based on the information held in said second coprocessor instruction execution flag and the result of the comparison by said second comparing circuit.

8. A processor system comprising:

a processor;

a coprocessor;

a shared memory connected to said processor and said coprocessor; and

a synchronous signal producing circuit for synchronizing access by said processor and said coprocessor to said shared memory, wherein

said synchronous signal producing circuit includes:

an access inhibit region register for designating an access inhibit region for said processor in said shared memory;

a comparing circuit for detecting the access by said processor to said access inhibit region designated in said access inhibit region register; and

a first logic circuit for issuing a signal setting said processor to a wait state based on a signal indicating that said coprocessor is executing a coprocessor instruction as well as a result of the comparison by said

comparing circuit.

9. The synchronous signal producing circuit according to claim 8, wherein

said first logic circuit issues the signal setting said processor to the wait state based on the signal indicating that said coprocessor is executing the coprocessor instruction, the result of the comparison by said comparing circuit and a signal indicating that locking of said shared memory is to be released.

10. The synchronous signal producing circuit according to claim 8, further comprising:

a bus wait counter for counting the number of bus wait cycles; and

a second logic circuit for issuing a bus error signal to said processor based on the signal indicating that said coprocessor is executing the coprocessor instruction, the result of the comparison by said comparing circuit and a count value of said bus wait counter.

11. The synchronous signal producing circuit according to claim 8, further comprising:

a first initial value register for setting a wait number at the time when the signal issued by said first logic circuit sets said processor to the wait state;

a second initial value register for setting a wait number at the time of normal access by said processor;

a selector for selecting the values in said first and second initial value registers based on the signal indicating that said coprocessor is executing the coprocessor instruction as well as the result of the comparison by said comparing circuit; and

a bus wait counter for receiving the value selected by said selector, and issuing a bus error signal to said processor when said bus wait counter counts the selected value.

12. The synchronous signal producing circuit according to claim 8, further comprising:

a third logic circuit for issuing a signal setting said processor to a low power consumption mode based on the signal indicating that said coprocessor is executing the coprocessor instruction as well as the result of the comparison by said comparing circuit.

13. The synchronous signal producing circuit according to claim 8, further comprising:

a coprocessor instruction execution flag for holding information indicating that the said coprocessor is executing the coprocessor instruction, wherein

said first logic circuit issues a signal for setting said processor to the wait state based on the information held in said coprocessor instruction execution flag and the result of the comparison by said comparing circuit.

14. The synchronous signal producing circuit according to claim 13, wherein

said access inhibit region register includes a first access inhibit region register for designating a first access inhibit region for said processor in said shared memory, and a second access inhibit region register for designating a second access inhibit region for said processor in said shared memory

said comparing circuit includes a first comparing circuit for detecting the access by said processor to said first access inhibit region designated in said first access inhibit region register, and a second comparing circuit for detecting the access by said processor to said second access inhibit region designated in said second access inhibit region register;

said coprocessor instruction execution flag includes a first coprocessor instruction execution flag for holding information indicating that the said coprocessor is executing the coprocessor instruction, and a second coprocessor instruction execution flag; and

said first logic circuit includes a second logic circuit issuing a signal

for setting said processor to the wait state based on the information held in said first coprocessor instruction execution flag and the result of the comparison by said first comparing circuit, and a third logic circuit issuing a signal for setting said processor to the wait state based on the information held in said second coprocessor instruction execution flag and the result of the comparison by said second comparing circuit.

15. A method of producing a synchronous signal for synchronizing access by a processor and a coprocessor to a shared memory, comprising the steps of:

designating an access inhibit region for said processor in said shared memory;

detecting the access by said processor to said designated access inhibit region; and

producing a signal setting said processor to a wait state based on a signal indicating that said coprocessor is executing a coprocessor instruction as well as a result of said detection.

16. The method of producing the synchronous signal according to claim 15, wherein

said step of producing the signal setting said processor to the wait state produces said signal setting said processor to the wait state based on the signal indicating that said coprocessor is executing the coprocessor instruction, said result of the comparison and a signal indicating that locking of said shared memory is to be released.

17. The method of producing the synchronous signal according to claim 15, further comprising the steps of:

counting the number of bus wait cycles; and

issuing a bus error signal to said processor based on the signal indicating that said coprocessor is executing the coprocessor instruction, said result of the comparison and said bus wait cycle number.

18. The method of producing the synchronous signal according to claim 15, further comprising the steps of:

setting a wait number at the time when said signal setting said processor to the wait state sets said processor to the wait state;

setting a wait number at the time of normal access by said processor;

selecting said set wait number at the time when said processor attains the wait state and said set wait number at the time of normal access by said processor based on the signal indicating that said coprocessor is executing the coprocessor instruction as well as said result of the detection; and

counting waiting cycles, and issuing a bus error signal to said processor when the number of the counted wait cycles reaches said selected value.

19. The method of producing the synchronous signal according to claim 15, further comprising the step of:

issuing a signal setting said processor to a low power consumption mode based on the signal indicating that said coprocessor is executing the coprocessor instruction as well as said result of detection.

20. The method of producing the synchronous signal according to claim 15, further comprising the step of:

holding information indicating that the said coprocessor is executing the coprocessor instruction, wherein

said step of producing the signal setting said processor to the wait state produces said signal setting said processor to the wait state based on said held information and said result of detection.